Embedded Capacitors

Presented by John Andresakis
VP of Strategic Technology
Oak-Mitsui Technologies
11-05
Agenda

- Overview of Embedded Capacitance
- Materials
- Product Design
- PWB Manufacturing Process
- Testing
- Selection Process
- Summary
Background / Motivation

High speed computing boards
Servers, Routers, Super computers

- CPU processor speed
- Operation voltage
- Power consumption

Power distribution improvement

Embedded capacitor

Module boards
Cell phones, PDA, Note book computers

- Multiple band
- More functions
- Cost

Miniaturization / HDI

Embedded capacitor
Background of demand for PCB with Embedded Capacitor

Voltage is decreasing

Allowable $\Delta V$ is $\pm 5\%$ of Voltage

$\Delta V = I^* R + I^* \frac{di}{dt}$

Will increase as clock speed increase

Will increase as Power increase

“Thin” power ground plane is the key parameter to improve electrical performance at high frequency!
Background of demand for PCB with Embedded Capacitor

Component density is reaching its limit

Source: Richard Ulrich University of Arkansas
Capacitor Usage by Function and Value

- **Timing**: 6.12%
- **Filter**: 30.23%
- **AC Coupling**: 13.22%
- **Energy Storage**: 2.02%
- **Reference**: 0.20%

# of Capacitors: 450Bn

**Decade Range**:
- ≤ 10 pf
- 100 pf
- 1000 pf
- 0.01 µf
- 0.1 µf
- 1 µf
- 10 µf
- > 10 µf

Range for Planar Capacitors
They Can be Really Small!

0402 resistor:
- (It’s the same size as President Lincoln’s bow tie)

Now find the 0201 capacitor:

Is there really such a thing as an 01005?:

Now inspect 2000 parts like this on one board

- Concern over Placement, Tombstoning, etc.
- Still need Vias for connecting

Courtesy of R. Snogren
The Embedded Capacitance Solutions

High speed computing boards
Servers, Routers, Super computers

Power distribution improvement

Module boards
Cell phones, PDA, Note book computers

Miniaturization / HDI

Ultra-Thin substrate
for use as embedded capacitor

Copper Foil
8~24 micron
Polymer Dielectric

Hi-Dk RCF
for used as embedded capacitor

Copper Foil
16 micron Polymer
Dielectric with
Hi-Dk Filler

Note: Manufacturing and use of Distributed (planar) Capacitance requires review of existing patents in the field including those of Sanmina-SCI.
Embedded Capacitance – Planar Construction

(NEMI Roadmap)
Planar Capacitance

- Parallel planes – a very simple idea

\[ C = \frac{A \cdot D_k \cdot K}{t} \]

Where:

- \( C \) = Capacitance (Farads)
- \( A \) = Area of plates
- \( D_k \) = Dielectric constant of material between plates
- \( K \) = Constant
- \( t \) = Thickness between plates
Planar Capacitor Materials
Ultra-Thin Substrates for use as Power Distribution Layers

Construction of ultra-thin substrate

- Copper Foil
- Dielectric layer 8 to 24 um
- Copper Foil
Planar Capacitance

- Material Sets
  - Capacitance layers (power and ground)
  - Thin Organic dielectrics
    - Epoxy-fiber glass (FR-4)
    - Modified Epoxy Film
    - Epoxy filled with BaTiO₃
    - Polyimide Film
    - Polyimide filled with BaTiO₃
    - Proprietary resins
  - Thin Inorganic dielectrics
    - Paraelectrics
    - Ferroelectrics
Planar Material Suppliers

- **Organic (thick-film)**
  - Sanmina-SCI – BC 2000, BC1000 (Licensed*)
  - Oak-Mitsui – FaradFlex (Licensed*)
  - DuPont – Interra HK (Licensed*)
  - 3M- C-Ply

- **Inorganic (thin-film)(in Development)**
  - Xanodics- Anodized Tantalum (paraelectric)
  - Rohm & Haas (Shipley)- Insite (ferroelectric)
  - Dupont- Barium Titanate (ferroelectric)
  - Motorola- “Gen 3” (ferroelectric)

*Note: Embedded Distributed Capacitance is a Patented Process. Not all materials shown are licensed for this application. They are shown for completeness. Please consult the material supplier about this matter.*
Sanmina-SCI
(BC 2000™)

- Benchmark for Embedded Planar Capacitance
  - Material supplied by most major Laminators
  - Capacitance density 506pF/in² [78 pF/cm²]
  - High Tg (170°C) epoxy resin with 106 fiberglass
  - Thin dielectric (0.002” [50 µm])
  - Hi-Pot testing voltage 500 VDC
  - 0.5, 1 or 2 oz Cu foil (Double treat or Reverse Treat Foil)
  - Patent Portfolio around the Materials and Use of Embedded Planar Capacitance

*Example: 1 layer pair on a 16”X20” board will produce about 146 nF; 7 layer pairs will approach the mF range.*

Note: BC2000 is a trademark of HSCI (Sanmina-SCI Corp)
Oak-Mitsui (FaradFlex®)

- **BC 8,12,16,24**
  - Modified Epoxy Film dielectric
  - Dk 4.4
  - Hi-pot tested to 500 VDC
  - Capacitance Density up to 480 pF/cm²

- **BC12TM, BC16T**
  - Filled (with High Dk particles) Modified Epoxy Film Dielectric
  - BC12TM- Dk 10, BC16T- Dk 30
  - Hi-pot Tested to 500 VDC for BC12TM, 100 VDC for BC16T
  - Capacitance Density up to 1700 pF/cm²
# Oak-Mitsui Embedded Capacitor Material Characteristics

<table>
<thead>
<tr>
<th>Properties</th>
<th>Method</th>
<th>BC24</th>
<th>BC16</th>
<th>BC12</th>
<th>BC8</th>
<th>BC12TM</th>
<th>BC16T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Thickness, µm</td>
<td>Nominal</td>
<td>24</td>
<td>16</td>
<td>12</td>
<td>8</td>
<td>12</td>
<td>16</td>
</tr>
<tr>
<td>Cp@ 1MHz, nF/in²(pF/cm²)</td>
<td><a href="2.5.5.3">IPC TM-50 2.5.5.3</a></td>
<td>1.0 (155)</td>
<td>1.6 (250)</td>
<td>1.9 (300)</td>
<td>3.1 (480)</td>
<td>4.5 (700)</td>
<td>11 (1700)</td>
</tr>
<tr>
<td>Dk @1MHz</td>
<td><a href="2.5.5.3">IPC TM-50 2.5.5.3</a></td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
<td>10</td>
<td>30</td>
</tr>
<tr>
<td>Loss Tangent @ 1 MHz</td>
<td><a href="2.4.9">IPC TM-50 2.4.9</a></td>
<td>0.015</td>
<td>0.015</td>
<td>0.015</td>
<td>0.016</td>
<td>0.019</td>
<td>0.019</td>
</tr>
<tr>
<td>Peel Strength, lbs/in</td>
<td><a href="2.5.6.3">IPC TM-50 2.5.6.3</a></td>
<td>&gt;8</td>
<td>&gt;8</td>
<td>&gt;8</td>
<td>&gt;8</td>
<td>&gt;4</td>
<td>&gt;6</td>
</tr>
<tr>
<td>Dielectric Strength, kV/mil</td>
<td><a href="D-882A">ASTM D-882A</a></td>
<td>5.3</td>
<td>7.3</td>
<td>5</td>
<td>5</td>
<td>6.2</td>
<td>2.8</td>
</tr>
<tr>
<td>Tensile Strength, Mpa (ksi)</td>
<td><a href="D-882A">ASTM D-882A</a></td>
<td>152(22.0)</td>
<td>164(23.8)</td>
<td>194(28.2)</td>
<td>126(18.3)</td>
<td>110(16.0)</td>
<td>NA</td>
</tr>
<tr>
<td>Elongation, %</td>
<td><a href="D-882A">ASTM D-882A</a></td>
<td>18.5</td>
<td>16.5</td>
<td>11.5</td>
<td>8.5</td>
<td>6.0</td>
<td>NA</td>
</tr>
<tr>
<td>CTE, ppm/°C</td>
<td>TMA</td>
<td>14 / 23</td>
<td>14 / 23</td>
<td>14 / 23</td>
<td>16 / 28</td>
<td>16 / 38</td>
<td>NA</td>
</tr>
<tr>
<td>Boil test, 2hrs Boil in water, 20 sec dip @260°C solder (10spec)</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td></td>
</tr>
<tr>
<td>Thermal Stress (20Sec Float @288°C), Times</td>
<td>-</td>
<td>&gt;10</td>
<td>&gt;10</td>
<td>&gt;10</td>
<td>&gt;10</td>
<td>&gt;10</td>
<td>&gt;10</td>
</tr>
<tr>
<td>Migration, 85C/85%RH/DC 35V</td>
<td>-</td>
<td>&gt;1000</td>
<td>&gt;1000</td>
<td>&gt;1000</td>
<td>&gt;1000</td>
<td>&gt;1000</td>
<td>&gt;1000</td>
</tr>
<tr>
<td>Flammability/Temp Rating</td>
<td>UL-94/ UL746</td>
<td>V0 130°C</td>
<td>V0 130°C</td>
<td>V0 130°C</td>
<td>V0 Pending</td>
<td>V0 130°C</td>
<td>V0 130°C</td>
</tr>
<tr>
<td>PWB Processing</td>
<td>Both side etching</td>
<td>Both side etching</td>
<td>Both side etching</td>
<td>Both side etching</td>
<td>Both side etching</td>
<td>Both side etching</td>
<td>Sequential Lamination</td>
</tr>
</tbody>
</table>

NA=Not Applicable
Oak-Mitsui
Embedded Planar Capacitor Example
Server Board

Capacitor Core

24 Layer Board
DuPont (Interra)

- **HK 4**
  - Polyimide film dielectric
  - 25 µm, Dk 3.5
  - Capacitance density 800 pF/in² (122 pF/cm²)
  - Hi-pot tested to 500 VDC

- **HK 11**
  - Filled Polyimide Film Dielectric
  - 14 µm, Dk 11
  - Capacitance Density 4500 pF/in² (698 pF/cm²)
  - Hi-pot Tested to 100 VDC
DuPont HK4
3M
(C-Ply)

- Epoxy dielectric filled with BaTiO$_3$
  - Un-reinforced
  - 0.16 to 1 mil [4 to 25 µm] thick (16 µm in commercialization)
  - Clad with 1oz copper (other weights available)
- Capacitance range:
  - 5 to 30 nF/in$^2$ [0.78 to 4.65 nF/cm$^2$]
  - Dk 15 – 23 (16 µm in commercialization)
- Hi-pot tested to 100 VDC
3M C-PLY

Pair of C-Ply cores on a sub-composite

Adjacent C-Ply cores

Single C-Ply core
Thin Film Paraelectrics - Technology

- SiO₂ 3.7  SiO 6  SiN 8  Al₂O₃ 9
- Ta₂O₅ 23  TiO₂ 40  Nb₂O₅ 40

- 0.1 - 2 µm thick
- 10 - 300 nF/cm²

- Sputtered, anodized

Pros
- Sputtering and anodization old, established techniques
- Capacitance density can be high since films can be very thin
- Stable with frequency, temperature, thickness
- Lowest parasitic inductance since thinnest dielectric

Cons
- Defect density can be sensitive to underlying metal roughness
- Delicate with regard to mechanical stress since thin
- May not pass ESD
- Lower Dielectric Strength (Breakdown Voltage)
- Vacuum processing
Thin Film Paraelectrics - Products

- **Rohm & Haas (Shipley) - InSite™**
  - SiO_x
  - 10 - 15 nF/cm²

- **Xanodics - Stealth™ Capacitor**
  - anodized Ta₂O₅
  - k = 23, 1000 Å, 200 nF/cm²
Ferroelectrics - Technology

- $k = 1000 \text{ to } 20,000$
- $1 - 10 \mu m$
- $100 - 2000 \text{ nF/cm}^2$

- Barium Titanate, Barium Strontium Titanate, Lead Zirconate Titanate, etc

- Sputtered, sol-gel, CVD, MOCVD or thick film precursor
- Cured at $>600^\circ C$ in oxygen

- Pros
  - Capacitance density can be very high
  - Parasitic inductance can be low since thin dielectric

- Cons
  - Requires $>600^\circ C$ cure, not directly processible on organic substrates
  - Can be expensive
  - Capacitance varies with $T$, frequency, voltage, thickness
Ferroelectrics - Products

- DuPont - Interra™
  - BaTiO₃ Thin Film on Copper
  - Under Development

- Rohm &Haas with Energenius - InSite™
  - “S3” Under development
  - PZT sol-gel
  - 200 nF/cm² reported

- Motorola
  - “Gen 3”
  - PZT sol-gel
  - Under Development
Capacitor Process Flow

- Design
  - Tools
  - Guidelines and work-arounds
- Simulation
- Manufacturing
  - Capital investment
  - Processing
- Test
Designing Capacitors
Capacitance

Parallel plates – separated by a dielectric

\[ C = \frac{A \cdot D_k \cdot K}{t} \]

Where:
- \( C \) = Capacitance (Farads)
- \( A \) = Area of plates
- \( D_k \) = Dielectric constant of material between plates
- \( K \) = Constant (8.85 pF/m)
- \( t \) = Thickness between plates

Capacitance/unit area (C/A)
- In nF/in\(^2\) = 0.2247Dk / t (where t is in mils)
- In nF/cm\(^2\) = 0.885Dk / t (where t is in microns)
P & G Plane Layer Pair

- Measure total overall (common/overlapping) copper plane area
- Subtract the sum of the areas of all via clearances, cut outs and any non copper features
- The result is the total conductor area or the total effective electrode area of the capacitor
- Multiply the above area by the capacitance density
- Be sure to use the same units of area measurement
- If more capacitance is required, more planes may be used and/or added specifically for capacitance

**IMPORTANT NOTE**: Due to decreased inductance the total capacitance needed with embedded capacitors is usually significantly less than when using discrete capacitors.
Planar Capacitors

- Assumptions
  - Parallel plate, single layer capacitors
  - Dielectric thickness and Dk are constant for a given material
  - Sizing calculations are based on material supplier reported capacitance density
  - Termination and clearance based on PWB manufacturers registration guidelines
  - Capacitance tolerances based on material supplier reported capacitance density variance and PWB manufacturers etch tolerance
Design Impact

- Capacitor removal
  - Rules need to be developed for specific system and processor speed
    - Many tests have been run showing that small value (fast response) decoupling capacitors can be entirely removed with ultrathin materials.

- Plane Clearances
  - Ultrathin low Dk materials
    - The plane clearances need to be strongly considered
      - Making cross board plane splits in a line, can create folding issue
      - Large clearances in both sides of material (ex. high voltage board areas) are to minimized. Hurts handling, increases damage chances, and may hurt registration
Design Impact

- **Plane clearances**
  - Ultrathin High Dk materials
    - Special processes used on this material make it less susceptible to plane clearance design approaches.

- **Use in power distribution**
  - Carefully select material when using high voltages
    - Insure adequate breakdown voltage and Hi-Pot survivability
    - Filled materials are designed for low voltage applications
Design Impact

- Use with high speed circuits
  - These materials are intended for high capacitance, not controlled impedance or low loss.
    - Most of the materials have good electrical properties, but not all.
      - Impedance control across these materials would be reduced
      - Conductor loss would be increased
      - Use of these materials for P/G planes reduces/eliminates this issues
  - High Dk materials would have negative impact on propagation velocity
  - Some materials are lossy, which is good for noise reduction, but very poor for transmission lines.
Power/Ground Plane Simulation

- Utilize EMI Stream
  - Developed by NEC
  - Based on SPICE Model
- Input PCB Layout in Design Format (.dsn file)
  - Output provide by standard design tools (Mentor Graphics, Cadence, etc.)
- Select thickness, Dk and Cu thickness of P/G planes
- Select frequency range
- Can add/subtract discrete SMT capacitors
- Other Software Available (ex. Sigrity)
Resonance Distribution

35- 0.1\( \mu \)F caps for power supply

Can not place caps!

35- 0.1\( \mu \)F caps for power supply
+44-0.1 \( \mu \)F caps for resonances

0.4mm (16 mil P/G)

24 \( \mu \)m P/G
Dk 4.4
No additional caps

Simulations provided by TechDream, Inc
Resonance Distribution- Lower Noise Threshold

-26 dB

400 µm (16 mil P/G)
79 caps

24 µm P/G
Dk 4.4
35 caps

12 µm P/G
Dk 10
35 caps
Frequency Response - Effect of Thickness, Dk

- **Dk-4.4**
- **Dk-10**
- **Dk-30**
Process Flow for Embedded Distributed Capacitance

• Select PCB Design as Candidate
  – Known problem with P/G noise, EMI
  – High pF Capacitor density
• Provide .dsn file for Simulation
• Set-up and run Simulation
• Build Prototype based on Simulation
• Analyze Prototype and Finalize design
Manufacturing Processes
Process Impact

- **Thin (25-50 µ) low Dk material (ZBC ™)**
  - Very little process impact for thin core capable suppliers
- **Ultrathin (<20 µ) low Dk materials (Oak-Mitsui-FaradFlex, DuPont HK-4, others)**
  - These materials are similar to thin flex circuit materials
  - These are normally “self supporting” materials
    - The dielectric material is strong enough to support itself through the PCB manufacturing process
  - Excellent thin core handling capability required by fabricator
  - Need to avoid folding lines (areas clear of copper)
- **Ultrathin (<20 µ) High Dk materials (Oak-Mitsui BC16T, 3M C-Ply, Dupont HK-11)**
  - These materials are normally not “self supporting”
  - In addition to excellent thin core handling capability, these materials require the use of special processing methods to manufacture the PCB.
1. Pre-clean  
   - Standard process

2. Expose Image  
   - Standard process

3. Dry Film lamination  
   - Standard process

4. Pattern etching  
   - Thin core compatible line recommended  
     Ex) Thin core Schmid etching line  
   - Use leader board if not confident  
   - Careful Handling required

5. Black oxidizing or alternative oxides  
   - Thin core compatible line recommended  
   - Use leader board if not confident  
   - Horizontal line preferred  
   - Careful Handling required

Important
Wet Process Equipment

Standard Line

Ultra flex line

Courtesy of Schmid
Handling Guidelines

Hold panel from 2 edges

Prevent holding panel from sides

Prevent holding panel with one hand
Planar Materials Not Requiring Sequential Lamination

- Typically Unfilled materials
- Material becomes a standard core in a MLB structure
- Does require scale characterization
- Thin Material Processing Equipment Required
Sequential Lamination

- Required for Most Filled Product
- Required for Thin Film Products
- Two passes through Inner layer Processing
Testing
Testing PWBs with Embedded Planar Capacitors

High Potential (HiPot) testing is performed on every image of an etched core.

- Flying probe testers measure capacitance for phase testing continuity and isolation of nets in PCBs.
- Software and Hardware modifications of “Bed of Nails” Tester is often required.
- Need to take into account the charging and discharging of the planes.
Power Bus Noise (UMR)

(Time Domain - 50 MHz)

Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00
Material Characterization

MEASURE $S_{21}$ BY DIRECT STIMULUS INJECTION INTO THE COPPER PLANES

4 LAYER TEST BOARD CROSS SECTION VIEW

VIA HEIGHTS REMAIN CONSTANT FOR ALL DLUT THICKNESS

VNA PORT 1

VNA PORT 2

FILLER PREPREG

DIELECTRIC LAYER

UNDER TEST

FILLER PREPREG
Power/Ground Self Impedance

Impedance magnitude [ohm]

Data courtesy of Istvan Novak Sun Microsystems
Transfer Impedance

Data courtesy of Istvan Novak Sun Microsystems
### PCB Electrical Performance

**Panel Size:** 50 in²
80% Retained Cu

<table>
<thead>
<tr>
<th>Product</th>
<th>nF</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZBC2000</td>
<td>16</td>
</tr>
<tr>
<td>ZBC1000</td>
<td>32</td>
</tr>
<tr>
<td>BC24</td>
<td>40</td>
</tr>
<tr>
<td>BC16</td>
<td>64</td>
</tr>
<tr>
<td>BC12</td>
<td>76</td>
</tr>
<tr>
<td>BC8</td>
<td>124</td>
</tr>
<tr>
<td>BC12T M</td>
<td>180</td>
</tr>
<tr>
<td>BC16T</td>
<td>440</td>
</tr>
</tbody>
</table>
PCB Electrical Performance
(Up to 1 GHz)

Panel Size = 50 in²
80% Retained Cu

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<tr>
<th>Product</th>
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</tr>
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</tr>
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<td>124</td>
</tr>
<tr>
<td>BC12T M</td>
<td>180</td>
</tr>
<tr>
<td>BC16T</td>
<td>440</td>
</tr>
</tbody>
</table>
PCB Electrical Performance
(Up to 3 GHz)

Panel Size= 50 in²
80% Retained Cu

<table>
<thead>
<tr>
<th>Product</th>
<th>nF</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZBC2000</td>
<td>16</td>
</tr>
<tr>
<td>ZBC1000</td>
<td>32</td>
</tr>
<tr>
<td>BC24</td>
<td>40</td>
</tr>
<tr>
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<td>64</td>
</tr>
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<td>76</td>
</tr>
<tr>
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</tr>
<tr>
<td>BC12T M</td>
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</tr>
<tr>
<td>BC16T</td>
<td>440</td>
</tr>
</tbody>
</table>
PCB Electrical Performance
(Thin versus High Dk)
Significant noise reduction on PWBs using thin capacitor layer

Difficult frequency range to reduce noise by discrete components

Conducted emission noise (dBEV)

Frequency of noise (MHz)

*Courtesy of Hitachi Ltd
Radiated Emissions Comparison

Close-Field Radiation J501-J603

Relative radiation field [dB]

-4.0E+01
-4.0E+01
-1.0E+02
-1.0E+02

Frequency [Hz]

1.00E+06 1.00E+07 1.00E+08 1.00E+09

2 mil
1 mil
0.3 mil

Bare board

Impedance and EMC Characterization

APEX '01
January 2001
Success Stories

- **High Speed Digital (Multiple Companies)**
  - Simplified Lay-out
  - Removed over 800 Caps on one design
  - Improved Electrical Performance
  - Improved EMI

- **IC Testers (Multiple Companies)**
  - Improved Electrical Performance
  - Maintained Board Thickness with added layers

- **Cable Infrastructure**
  - Removed most caps- able to do single sided assembly
  - Reduced board size
  - Maintained board thickness
Discrete Capacitor
Discrete Material Suppliers

- Materials used for Planar Capacitors

- Paste Materials
  - Dupont- Ceramics- Fired at high temperature
  - Huntsman- Photosensitive Polymer filled with High DK powder (Motorola Mezzanine Capacitor)
  - Hitachi- Thermal Cured Polymer filled with High Dk powder

- Resin Coated Foil
  - Oak-Mitsui MC16TR
Hi-Dk RCF Material Construction

**Characteristics**

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Condition</th>
<th>Unit</th>
<th>BC16TR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance</td>
<td>1MHz</td>
<td>pF/cm²</td>
<td>1,700</td>
</tr>
<tr>
<td>Dk</td>
<td>1MHz</td>
<td>N/A</td>
<td>30</td>
</tr>
<tr>
<td>Df</td>
<td>1MHz</td>
<td>N/A</td>
<td>0.019</td>
</tr>
<tr>
<td>Dielectric Thickness</td>
<td>Nominal</td>
<td>Micron Meter</td>
<td>16</td>
</tr>
<tr>
<td>Peel Strength</td>
<td>IPC TM-650 2.4.9</td>
<td>kN/m</td>
<td>&gt;0.7</td>
</tr>
<tr>
<td>Thermal Stress</td>
<td>20sec @288°C</td>
<td>times</td>
<td>&gt;10</td>
</tr>
<tr>
<td>Electrical Migration</td>
<td>85C/85%RH/35V</td>
<td>hrs</td>
<td>&gt;1000</td>
</tr>
</tbody>
</table>
Designing Embedded Capacitance Board Geometry and Capacitance (Example)

40 capacitors ranging from 1pF to 160pF in 10x10mm

Geometry calculated based upon 16µ Filled material: 1,700pF/cm²

Expected tolerance*
1 - 2pF  5 - 10%
2 - 10pF 3 - 5%
10 - 20pF 2 - 3%
20 - 100pF 1 -2%
100 - < 1%

*Based on electrode geometry definition +/- 10micron
“Discrete” Capacitor Process Using Resin Coated Foil
Removal of dielectric layer

Before sand blast process

Top view

Cross sectional

After sand blast process
Capacitance uniformity evaluation result

- Capacitor size: 50.8x50.8mm
- 192 measurement points
- Uniformity <5%

BC16TR
Approx. 44nF

Deviation from target value (%)

Frequency

Capacitor size: 50.8x50.8mm
50.8mm (2 inch)
648mm
470mm

50.8mm (2 inch)
Capacitance uniformity evaluation

144 module

100 capacitors in 1cm²
0.50 x 0.50mm

14,400 capacitor
Flying Probe LCR measurement of Embedded Passive Boards
Capacitance uniformity evaluation result

0.5 x 0.5mm Capacitor

Variation from mean value

Uniformity <7%

14,400 capacitor

Mean value: 4.25pF

$3\sigma = 6.7\%$
Success Story

- Motorola Cell Phone Modules
  - Utilize Screen Printed Pastes
  - Millions of Modules shipped
  - Significant savings/module
Further Studies

• Measure EMI from assembled boards and compare with Simulation results
• Conduct High Frequency testing on “Discrete” Embedded Capacitors
  – Test Vehicle Designed
  – Utilize Crane NAVSEA Facility
  – Test to 12 GHz
Crane Test Vehicles for High Frequency Testing

### Stackup 1 of 2 – Resin Coated Foils

<table>
<thead>
<tr>
<th>LAYER</th>
<th>TYPE</th>
<th>MATERIAL</th>
<th>THICKNESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SIGNAL</td>
<td>1/2 oz. COPPER</td>
<td>0.7</td>
</tr>
<tr>
<td>2</td>
<td>SIGNAL</td>
<td>Resin Coated Foil</td>
<td>*</td>
</tr>
<tr>
<td>2</td>
<td>GROUND</td>
<td>1/2 oz. COPPER</td>
<td>0.7</td>
</tr>
</tbody>
</table>

Board Features:
- 6 layers
- Does not require thin-core processing
- .006" laser microvias (Layers 1-2, 1-3, 4-6, 5-6)
- Nelco N4000-13 SI
- .030" thick
- Symmetrical
- 2 capacitive layers
- SMOBC, ENIG

* Dielectric thickness varies by material

### Stackup 2 of 2 – Thin Core Laminates

<table>
<thead>
<tr>
<th>LAYER</th>
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<th>THICKNESS</th>
</tr>
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<td>2</td>
<td>GROUND</td>
<td>1/2 oz. COPPER</td>
<td>0.7</td>
</tr>
</tbody>
</table>

Board Features:
- 6 layers
- Requires thin-core processing
- .006" laser microvias (Layers 1-2, 1-3, 4-6, 5-6)
- Nelco N4000-13 SI
- .031" thick
- Symmetrical
- 2 capacitive layers
- SMOBC, ENIG

* Dielectric thickness varies by material

[NAVSEA Logo]

[ECT Logo]
Crane Test Vehicles for High Frequency Testing

Capacitor Cross Section 1 of 2

Processing option 1 – Remove the unused capacitor dielectric material
- Capacitor is formed between layers 2 and 3
- Laser microvia connection gives low series inductance

Capacitor Cross Section 2 of 2

Processing option 2 – Unused capacitor dielectric material is not removed
- Capacitor is formed between layers 2 and 3
- Laser microvia connection gives low series inductance
Selection Criteria

- Capacitance
- Density/Inductance
- Operating Voltage
- PWB processes
- Cost/Performance
Capacitance Density

More Capacitance

ferroelectrics - 2000 nF/cm²
thin film paraelectrics - 300 nF/cm²
polymers filled with ferroelectric particles - 5 nF/cm²
thin unfilled polymers - 1.5 nF/cm²
thick unfilled polymers - 0.3 nF/cm²
Parasitic Inductance

Less Inductance

- thin film paraelectrics
- ferroelectrics
- thin unfilled polymers
- polymers filled with ferroelectric particles
- thick unfilled polymers

This is related to dielectric thickness
Cost (Roughly) - Per Unit Area

- Ferroelectrics
  - thin film paraelectrics
  - polymers filled with ferroelectric particles
  - thin unfilled polymers
  - thick unfilled polymers

Lower Cost
IPC Activities

- **Standards**
  - Embedded Capacitor Materials
    - IPC 4821 Ready for Publishing
  - Embedded Resistor Material
  - Embedded Passive Design
  - Embedded Passive Performance

- **IPC Expo 2006**
  - Sessions on Embedded Passives

- **IPC 3rd Embedded Passives Conference**
  - May 2-4 in Boston Area

- **IPC Embedded Devices Users Group**
  - Regular Teleconferences to discuss technology
Summary

- Embedded Capacitor Technology can improve system price/performance by:
  - Reducing discrete caps
  - Reducing PWB size/thickness
  - Increasing functionality
- Thinner power distribution planes are required for improved impedance performance at high frequency.
- New substrates have demonstrated excellent electrical performance and physical properties.
- They are compatible with PCB processing; a truly “drop in” material.
- Materials are commercially available from licensed fabricators.
- Substrates filled with ferroelectric particles have better performance, but result in higher cost PCBs.
Summary

• Simulation tools exist to help in determine effectiveness of Embedded Capacitors prior to prototyping.
• The use of Embedded Capacitance can simplify PCB lay-out and reduce the number of prototypes required.
• Discrete Capacitors can be formed using High Dk Resin Coated Foil or Pastes
• Design Tools exists to utilize Embedded Discrete Components
• Research is being conducted on high frequency response of Embedded “Discrete” Capacitors
• Many Success Stories for use of Embedded Passives
Thank You

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